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7590 10/27/2003

McDERMOTT, WILL & EMERY
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/053,543	01/24/2002	Masahiro Shimizu	57454-329	3990

TITLE OF INVENTION: INTEGRATED CIRCUIT HAVING A MEMORY CELL TRANSISTOR WITH A GATE OXIDE LAYER WHICH IS THICKER THAN THE GATE OXIDE LAYER OF A PERIPHERAL CIRCUIT TRANSISTOR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1330	\$300	\$1630	01/27/2004

EXAMINER	ART UNIT	CLASS-SUBCLASS
PERALTA, GINETTE	2814	438-197000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

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(B) RESIDENCE: (CITY and STATE OR COUNTRY)

RENESAS TECHNOLOGY CORP.

Tokyo, JAPAN

Please check the appropriate assignee category or categories (will not be printed on the patent); ☐ individual ☒ corporation or other private group entity ☐ government

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Stephen A. Becker, Reg. #26,527 1/27/2004

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